

ALISH KANANI

B.Tech, Electrical Engineering
Indian Institute of Technology Jodhpur
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EDUCATION

B.Tech - Electrical Engineering

IIT Jodhpur | CGPA:8.75/10

2017 – 2021

PUBLICATIONS

- I. Kool, A. Kanani, R. Bhattacharjya, "Approximating Communication Systems: Reality or Fantasy?" 28th IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC)- Student Research Symposium, Bangalore, India (Virtual Event), 2021. **Poster**
- A. Kanani, R. Bhattacharjya and D. S. Banerjee, "ApproxBioWear: Approximating Additions for Efficient Biomedical Wearable Computing at the Edge," 2021 43rd Annual International Conference of the IEEE Engineering in Medicine Biology Society (EMBC), 2021. **Paper**
- A. Kanani, S. Vaidya and H. Agarwal, "LightFPGA: Scalable and Automated FPGA Acceleration of LightGBM for Machine Learning Applications," 2021 25th International Symposium on VLSI Design and Test (VDAT), 2021. **Paper**
- A. Kanani, J. Mehta and N. Goel, "ACA-CSU: A Carry Selection Based Accuracy Configurable Approximate Adder Design," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, 2020. **Paper**
- R. Bhattacharjya, A. Kanani and N. Goel, "ReARM: A Reconfigurable Approximate Rounding-Based Multiplier for Image Processing," 24th International Symposium on VLSI Design and Test (VDAT), Bhubaneswar, India, 2020. **Paper**

EXPERIENCE

Hardware Engineer

Jul 2021 – Now

Imagination Technologies

- Working in Automotive Ethernet Packet Processing IP team.
- Day to day task involve RTL design and fixes, lint, cdc, synthesis, power analysis, equivalence check etc
- handling entire design flow, including all different tools, Jenkins Jobs, release flow etc
- Worked on ISO 26262 safety critical analysis.
- Worked on internal tool development (python based) for FMEDA (Failure modes, effects, and diagnostic analysis) which is being used in all automotive IPs.

FPGA Implementation of CRAFT Algorithm

May 2020 – Aug 2020

TCS Research & Innovation | Research Intern

- Suggested implementation methods to speedup CRAFT text detection network on Alveo FPGA.
- **3 to 100X** speedup achieved using different approaches.
- Learned **Vitis AI** and **HLS** for different kind of speedup technique.

Design Space Exploration of 8-bit Approximate Prefix Adders

May 2020 – July 2020

Vienna University of Technology (TU Wien) | Research Intern

Prof. Muhammad Shafique

- Proposed **1.4 Million** approximate adders from 4 different Prefix tree.
- Automated process to extract performance and error matrix for each configuration using **ABC synthesis tool** and **python**.
- Extracting all the **Pareto Optimal** adders using different performance and error matrix curve and assembling all the adders to make the library.

Accuracy Configurable Arithmetic Circuit

May 2019 – July 2019

IIT Ropar | Research Intern

Dr Neeraj Goel

- Studied various existing approximate binary adders and multipliers.
- Proposed **An Accuracy Configurable Adder** and helped in **An Accuracy-Configurable Rounding-Based Multiplier**.
- Compared proposed algorithms with state of the art algorithms using **Synopsys Design Compiler** and **octave**.

PROJECTS

LightFPGA : Acceleration of LightGBM by FPGA Implementation

Sep 2020 – Nov 2020

B.Tech Project

Guide: [Dr Harshit Agarwal](#)

- Automated the **Verilog** generation of decision tree-based [LightGBM](#) for FPGA implementation.
- Made the **LightFPGA** library in Python which performs all the required steps for Verilog Generation and testing form extracted LightGBM classification model.
- On Alveo u280 FPGA, around **700 to 1000X** speedup achieved for different data-sets.

DHVANIK - Wearable Tympanometric Diagnostic Tool for Middle Ear Ailments

Sep 2019 - Dec 2019

Inter IIT Tech Meet Competition

Guide: [Dr Arpit Khandelwal](#)

- Developed a low-cost, user-friendly, IoT enabled, head-phone sized **tympanometer** that detects middle ear problems.
- Made business model for IICDC 2019 and Inter IIT 2019.

Optimisation of 32 bit adders on FPGA

Jan 2019 - Apr 2019

B.Tech Project

Guide: [Dr S. P. Tiwari](#)

- Studied six different algorithms to add two binary numbers.
- Compared delay, area and power of these algorithms in **Xilinx-ise**.
- Project report and code: github.com/AlishKanani/32bitAdders/

AES Data Encryption on FPGA

Sep 2018 - May 2019

Gymkhana Project

- Developed an FPGA based encryption-decryption engine to facilitate speed up in AES encryption.
- Project link: github.com/AlishKanani/AES

NETRA- Indoor Navigator for Visually Impaired

Aug 2018 - May 2019

Texas Instruments IICDC Competition

Guide: [Dr Arpit Khandelwal](#)

- Applied dead reckoning for indoor navigation without expensive infrastructure.
- Implemented on **Beaglebone black** using 9 axis **IMU**.
- Audio and haptic feedback for navigation especially for the visually impaired.

TECHNICAL SKILLS

Programming Languages: Python • C • C++ • MATLAB • Perl(Basic)

HDL: Verilog • System Verilog • VHDL (Basic) • HLS

Softwares: ASIC Synthesis Tools (Synopsys DC & cadence genus) • Spyglass Lint and CDC • Simulation tools (VCS & XCELIUM) • Vivado • Vitis AI • Vitis HLS • codebeamer ALM tool

Others: Safety analysis • Deep Neural Network(Basic) • LaTeX • Arduino

RELEVANT COURSES

Digital Logic and Design
Microprocessors controllers
Analog Electronics
Circuit Theory

Communication Systems
Signals and Systems
Digital Signal Processing
Digital Image Analysis

Power Electronics
Power System
Control Systems
Sensors and Measurement

POSITIONS OF RESPONSIBILITY

Captain | Electronics Club

Aug 2018 – May 2019

Student Guide | Counselling Service

May 2018 – July 2019

ACHIEVEMENTS

- Presented poster on Approximate Multiplication at Research Conclave, IIT Guwahati.
- Presented a poster of DHVANIK on Industry Day, IIT Jodhpur.
- Secured **Bronze** medal in Inter IIT Techmeet 2019.
- Led the team of project NETRA and DHVANIK which reached the **semi-finals** of DST and Texas Instruments IICDC 2018 and 2019.
- Placed among the top 0.5% of 1.4 million applicants in JEE Advanced 2017.