ALISH KANANI

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SUMMARY

I am a first-year Ph.D. student at the University of Wisconsin-Madison, working on thermal modeling and management of 2.5D-3D architecture. I am being advised by Professor Umit Ogras, with a focus on advancing computer systems through innovative design and integration techniques. Previously, I worked in the semiconductor industry, as a system architect and RTL designer.

EDUCATION

Doctoral Student - Computer Systems and Architecture
University of Wisconsin-Madison, ECE Department | GPA:4/4   *2023 –*
Bachelor of Technology - Electrical Engineering
Indian Institute of Technology (IIT) Jodhpur | GPA:8.75/10   *2017 – 2021*

PUBLICATIONS

- Rajat Bhattacharjya, **Alish Kanani**, A Anil Kumar, Manoj Nambiar, M Girish Chandra, Rekha Singhal, "Ellora: Exploring Low-Power OFDM-based Radar Processors using Approximate Computing", 15th IEEE Latin American Symposium on Circuits and Systems (LASCAS), Punta Del Este, Uruguay, February 2024 **Paper**

- Ish Kool, **Alish Kanani**, Rajat Bhattacharjya, "Approximating Communication Systems: Reality or Fantasy?" 28th IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC)- Student Research Symposium, Bangalore, India (Virtual Event), 2021. **Poster**

- **Alish Kanani**, Rajat Bhattacharjya and Dip Sankar Banerjee, "ApproxBioWear: Approximating Additions for Efficient Biomedical Wearable Computing at the Edge," 2021 43rd Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC), 2021. **Paper**

- **Alish Kanani**, Swar Vaidya and Harshit Agarwal, "LightFPGA: Scalable and Automated FPGA Acceleration of LightGBM for Machine Learning Applications," 2021 25th International Symposium on VLSI Design and Test (VDAT), 2021. **Paper**

- **Alish Kanani**, Jigar Mehta and Neeraj Goel, "ACA-CSU: A Carry Selection Based Accuracy Configurable Approximate Adder Design," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, 2020. **Paper**

- Rajat Bhattacharjya, **Alish Kanani** and Neeraj Goel, "ReARM: A Reconfigurable Approximate Rounding-Based Multiplier for Image Processing," 24th International Symposium on VLSI Design and Test (VDAT), Bhubaneswar, India, 2020. **Paper**

WORK EXPERIENCE

Samsung Electronics   Aug 2022 – July 2023
Senior Engineer - System Architecture and Digital Design
- Worked on 3D IC test chip projects at Samsung's Foundry Business Unit.
- My projects included logic-logic and DRAM-logic 3D IC test chips, these vertically stacked chips were connected using thru silicon vias (TSVs)
- The work included system-level architecture discussion of these test chips and integration of IPs, I specifically worked on one-time programmable (OTP) memory controller responsible for repair (TSV, MBIST, etc), different on-chip performance counters and PCIe subsystem.

Imagination Technologies   Jul 2021 – Aug 2022
Hardware Engineer - Design Automation and RTL Design
- Worked in Automotive Ethernet Packet Processing IP (layer 2 switch and layer 3 routers) team.
- My Day-to-day tasks were RTL design and fixes, lint, CDC, synthesis, power analysis, equivalence check, etc.
- Handled entire design flow, including all different tools, Jenkins Jobs, release flow, etc.
- Worked on ISO 26262 safety critical analysis.
- Worked on internal tool development for FMEDA (Failure modes, effects, and diagnostic analysis) which was being used in all automotive IPs for automotive safety certification.

INTERNSHIPS

FPGA Implementation of CRAFT Algorithm   May 2020 – Aug 2020
TCS Research & Innovation | Research Intern
- Suggested FPGA-based different architectures and automated implementation of CRAFT, a CNN-based text detection algorithm on FPGA for real-time inference.
- **3 to 100X** speedup achieved using different approaches.
- Learned **Vitis AI** and **HLS** for different type of implementations.

Design Space Exploration of Approximate Prefix Adders   May 2020 – July 2020
Vienna University of Technology (TU Wien) | Research Intern   *Prof. Muhammad Shafique*
- Automated complete design space exploration to extract all possible approximate prefix adders from 4 different prefix trees, Kogge Stone, Brent Kung, Han Carlson and Ladner Fischer Adder.
- More than 1.4 Million adder configurations were generated (Verilog), tested, and synthesized, and the accuracy matrix was calculated using open source **ABC synthesis tool** and **python**.

Accuracy Configurable Arithmetic Circuit   May 2019 – July 2019
IIT Ropar | Research Intern   *Dr Neeraj Goel*
- Studied various existing approximate binary adders and multipliers.
- Proposed **An Accuracy Configurable Adder** and **An Accuracy-Configurable Rounding-Based Multiplier**.
- Compared proposed algorithms with state of the art algorithms using **Synopsys Design Compiler** and **octave**.

TECHNICAL SKILLS

Programming Languages: Python ● C ● C++ ● MATLAB ● Perl(Basic) ● Shell-Scripting
HDL: Verilog ● System Verilog ● VHDL (Basic) ● HLS
Softwares: Ansys Fluent ● ASIC Synthesis Tools (Synopsys DC & cadence genus) ● Spyglass Lint and CDC ● Simulation tools (VCS & XCELIUM) ● Vivado ● Vitis AI ● Vitis HLS ● codebeamer ALM tool
Others: Safety analysis ● Deep Neural Network(Basic) ● LaTex ● Git ● Arduino

ACHIEVEMENTS

- Employee of the Month for Apr-2023 at Samsung Electronics.
- Secured **Bronze** medal in Inter IIT Techmeet 2019.
- Led the team of project NETRA and DHVANIK which reached the **semi-finals** of DST and Texas Instruments IICDC 2018 and 2019 startup challenge.
- Placed among the top 0.5% of 1.4 million applicants in JEE Advanced 2017.